NEW HORIZON COLLEGE OF ENGINEERING

IEEE NHCE STUDENT BRANCH

IEEE PES Power & Energy Society® New Horizon College of Engineering, PE31 Student Branch Chapter

IEEE PES Power & Energy Society® BANGALORE CHAPTER

Guest Lecture

Verilog HDL for Digital Design Concepts and Applications

8th May 2026

10:00 AM to 12:00 PM

Room No. B 205

4th Semester EEE Students

Dr. Praveen Kumar Reddy
DFT Engineer
Truechip Technologies

Faculty Coordinators
Dr. M Karthika
Dr. P Meenakshi Sundaram

Convenor
Dr. S Sujitha
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Dr. R J Anandhi
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Principal

Organised by
Department of Electrical and Electronics Engineering

Department of Electrical and Electronics Engineering

IEEE Power and Energy Society

Event Report

Title	**Verilog HDL for Digital Design Concepts and Applications**	
Department	Electrical and Electronics Engineering	
Date	From: 8.05.2026	To: 8.05.2026
Time	From: 10:00 AM	To: 12:00 PM
Brief Description	The talk was conducted on the topic of Verilog HDL for Digital Design and VLSI Industry Insights, exclusively for 4th- semester EEE students. The session was handled by Dr. Praveen Kumar Reddy K, DFT Engineer, True Chip Technologies, Bangalore. A guest lecture on "Verilog HDL for Digital Design Concepts and Applications" was conducted to provide students with practical exposure to digital hardware design using Hardware Description Language (HDL). The resource person explained fundamental concepts of Verilog HDL including modules, data types, operators, combinational and sequential circuit design, flip-flops, counters, registers, and finite state machines. Different modeling styles such as behavioral, structural, and dataflow modeling were discussed with clear coding examples and circuit illustrations. The session was delivered in an interactive manner with effective explanations, enabling students to connect theoretical digital electronics concepts with practical hardware implementation techniques. The resource person shared insights on digital logic design, the evolution of chips as predicted by Moore's Law, and demonstrated Verilog HDL programmes on Half Adder, Full Adder, 2-to-4 Decoder, and Counters. He gave an overview of the current VLSI industry, the various roles available in the field, and explained the top-down and bottom-up approaches of chip design through relatable examples. **Key Takeaways:** • Understanding of digital logic design and the chip design process. • Evolution of semiconductors and Moore's Law. • Hands-on Verilog HDL programmes on basic digital circuits. • VLSI industry roles and career opportunities. • Top-down and bottom-up design methodologies. **Outcome of the Workshop:** • The participants gained practical knowledge in digital design and Verilog HDL, with a clearer understanding of VLSI career pathways, encouraging students to explore chip design beyond the curriculum. • The lecture improved students' technical skills, industry awareness, and interest in pursuing projects and careers related to digital design and VLSI technologies. The programme was organised by Dr Karthika M, Associate Professor and Dr Meenakshi Sundaram, Sr. Assistant Professor, EEE under PES IEEE SBC, NHCE, and 90 students of 4th semester were benefitted by the event.	

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